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(54) **Compound semiconductor field-effect transistor.**

(57) A field-effect transistor has two planar-doped layers (7,8), each having two-dimensionally doped impurities. The layers (7,8) extend in the channel region (5) between the source (3) and the drain (4), and are separated by a distance substantially equal to or less than the mean free path of electrons. The invention provides a field-effect transistor with high-frequency and high-speed operating characteristics.

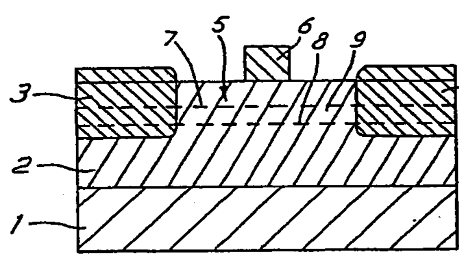

FIG.1

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Description

COMPOUND SEMICONDUCTOR FIELD-EFFECT TRANSISTOR

The present invention relates to a compound semiconductor field-effect transistor such as GaAs FET, InP FET or InGaAs FET, and more particularly to an atomic planar-doped field-effect transistor which has an atomic planar-doped layer in the channel region.

The compound semiconductor field-effect transistors are featured by their high carrier mobilities and high velocities in carrier saturation and have been widely employed as high-frequency discrete transistors or in high-speed IC devices. It is however demanded to further raise their operation frequencies and operation speeds. For that purpose, it is required to make the devise size smaller and the channel layer thinner, thereby increasing the transconductance while maintaining the gate-source breakdown voltage and the current driving capability. Schubert et al. have proposed the atomic planar-doped field-effect transistor to meet the requirements, in IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. ED-33, No. 5, May 1986, pp. 625-632. The proposed FET has such a planar-doped layer within its channel region between the source and the drain that is an atomic monolayer where ionized donors extend two-dimensionally. This structure realizes a thinned channel while maintaining the gate breakdown voltage.

In the proposed FET, however, ion scattering causes scattering of carrier electrons, which decreases the mobility at a low electric field. The decreased mobility at a low electric field causes an increase in the parasitic resistance of the device. Moreover, overshoot effect is decreased due to increase in ion scattering, and it is impossible to expect a substantial improvement of the characteristics even if a device size is lowered.

Ploog et al. have presented a solution of the above problems, in which the atomic planar-doped layer is separated from the electron channel by the use of a heterojunction, in Journal of Crystal Growth, Vol. 81, 1987, p.304. However, the use of a heterojunction gives rise to another problem that the device characteristics become unstable due to a deep level which is generally present in heterojunction devices.

It is an object of the present invention to provide a stable planar-doped field-effect transistor for high-frequency and high-speed operation in which the mobility at a low electric field is enhanced without using a heterojunction.

The planar-doped field-effect transistor according to the present invention is characterized by having two planar-doped layers in a channel region between source and drain. The two planar-doped layers, each formed by atomic-planar-doping, that is, by doping impurities two-dimensionally, are spaced at an interval substantially equal to or less than a mean free path of electrons.

In the structure of the present invention, a large majority of carrier electrons are present at a center of the interval between the two planar-doped layers, specially separated from the ionized donors at the planar-doped layers. Therefore, the carrier electrons are hardly affected by scattering of the impurity ions and the mobility at a low electric field is not reduced. Since the scattering due to the ion scattering is suppressed, the overshoot effect of saturation velocity of electrons appears in the device whose size is highly decreased. Thus, the operating speed is greatly improved and it is possible to realize an ultra-high-speed device.

Fig. 1 is a schematic sectional view of a planar-doped FET according to an embodiment of the present invention.

Fig. 2 is an enlarged view of an energy-band diagram at a channel region of the planar-doped FET shown in Fig. 1.

Fig. 3 shows the distributions of the carrier electron concentration and ionized donor concentration in the depthwise direction of the channel region of the planar-doped FET shown in Fig. 1.

Fig. 4 is an energy band diagram of a conventional planar-doped FET.

Fig. 5 is a partial, enlarged view of the energy-band diagram of Fig. 4 at a channel region of the conventional planar-doped FET.

Fig. 6 shows distributions of the carrier electron concentration and ionized donor concentration in the depthwise direction of a channel layer of the conventional planar-doped FET.

Referring to Fig. 1, the planar-doped field-effect transistor according to an embodiment of the present invention comprises a semi-insulating GaAs substrate 1, an undoped p^--GaAs epitaxial layer 2 formed on the substrate 1, a source 3 and a drain 4 formed on the epitaxial layer 2 and spaced apart from each other to leave a channel region 5 therebetween at the surface portion of the expitaxial layer 2, a gate electrode 6 of Aℓ, Ti-Aℓ or W-Si formed on the surface of the channel region 5, and two atomic planar-doped layers 7 and 8 formed within the channel region 5. The planar-doped layers 7 and 8 are formed through a conventional method by two-dimensionally doping impurity atoms such as Si, Se or S. The upper planar-doped layer 7 may be formed 100 to 500 Å below the surface of the channel region 5 and the interval between the two planar-doped layers 7 and 8, that is, a thickness of a portion 9 between the two layers 7 and 8, is for example 70 Å, about a mean free path of electron, or less. Each of the planar-doped layers 7 and 8 has a thickness substantially equal to a size of one atom of the doped impurity. Instead of GaAs semi-insulating substrate, InP semi-insulating substrate may be used, with an epitaxial layer thereon of InP or InGaAs in which two planar-doped layers of Si, for example, are formed.

A conventional planar-doped FET with a single planar-doped layer has an energy-band diagram as shown in Fig. 4 in which a conduction band 11 and a valence band 12 have V-shaped recesses at a

position where the single planar-shaped layer is formed. The V-shaped recess in the conduction band 11 acts as a potential well in which carrier electrons 19 exist locally in the vicinity of the ionized donors 17. The field strength near the gate electrode 6 is far smaller than in the case of uniform doping. Thus, it has become possible to minimize the thickness of the channel region while maintaining the gate breakdown voltage. Referring to Fig. 5, which is an enlarged view of the V-shaped potential well portion in Fig. 4, electrons have quantized energy levels E_0, E_1, E_2 ..., and the existing probabilities ($\Psi \bullet \Psi^*$) 14 of carrier electrons have a peak at the same spatial location of the ionized donors 17. The distribution of carrier electron concentration is shown in Fig. 6 wherein the axis of abscissas represents the channel depth and the axis of ordinate represents the carrier electron concentration 114 and ionized donor concentration 117. As will be clear from Fig. 6, the distribution 114 of carrier electrons is at the same location as that 117 of the ionized donors, that is, the location X_0 of the planar-doped layer, and therefore scattering due to ion scattering increases and the mobility at low electric field lowers. However, it has heretofore been considered that, since the transconductance of a very small FET having a channel length of 1 µm or less is determined by a velocity Vs in electron saturation and the channel depth, the decrease in the mobility at low electric field due to ionized impurity scattering gives rise to no problem in regard to the device characteristics. However, there is a problem that a lowered mobility at low electric field causes an increase in the parasitic resistance of the device. There is another problem that, if ion scattering increases, overshoot effect decreases and it is impossible to expect a substantial improvement in the characteristics even if miniaturization is achieved.

Referring now to Fig. 2, the conduction band 21 at the channel region 5 (Fig. 1) of the transistor of the invention has a recessed potential well portion with a flat bottom between the locations of the ionized donors 27 and 28, that is, the locations of the two planar-doped layers 7 and 8 whose depths are X_1 and X_2, respectively, as shown in Fig. 3.

The recessed potential well portion has the quantized energy levels E_0, E_1, E_2, ... and the existing possibilities of carrier electrons ($\Psi \bullet \Psi$) are indicated by 24. A large majority of the carrier electrons exist in the ground state E_0 and particularly at the center of the interval ($X_2 - X_1$) between the two planar-doped layers 7 and 8. The distribution 124 of the carrier electrons and the distributions 127 and 128 of the ionized donors 27 and 28 are shown in Fig. 3 whose absissa represents the channel depth. As is clear from Fig. 3, a greater part of carrier electrons are spatially separated from the ionized donors, and hence the effect of Coulomb scattering of the donor ions upon the carrier electrons is suppressed and there is no lowering in the mobility at a low electric field.

EMBODIMENT 1

On a semi-insulating GaAs substrate 1 (Fig. 1), an undoped p⁻-GaAs layer (a part of 2 below 8) was grown by the molecular beam epitaxy (MBE) method to a thickness of 0.8 µm. The layer 2 because P⁻-type spontaneously, with an impurity (mainly carbon) concentration of 1×10^{-14} cm^{-3}. When the thickness reached 0.8 µm, the fluxing of Ga in MBE was stopped and fluxing of Si was initiated for such a period of time that a sheet density of 1×10^{-12} cm^{-2} Si was achieved, thereby forming the lower planar-doped layer 8. Then, the fluxing of Si was replaced by that of Ga and a P⁻-GaAs layer 9 was grown to a thickness of 70 Å. The fluxing of Ga was again stopped and fluxing of Si was applied for such a period of time that a sheet density of 1×10^{-12} cm^{-2} was achieved, thereby forming the upper planar-doped layer 7. Thereafter, a P⁻-GaAs layer (the upper part of 2 above 7) was grown to a thickness of 300 Å. Then, a gate electrode 6 having a gate length of 0.5 µm was formed of Aℓ. At the portions intended for source and drain, AuGe alloy and then Ni were deposited and they were alloged at 450°C to form source and drain ohmic electrodes 3 and 4. The distances between the edges of the source and drain and the opposing edges of the gate were 1 µm, respectively.

The Hall measurement was conducted for the completed transistor and the result showed that the mobility was 4000 cm^2 / V.sec, which was considerably higher than the value of a conventional transistor. Moreover, it was revealed that the cut-off frequency was 35 GHz, which was closer to the value of a heterojunction high-mobility transistor beyond the value 20 GHz of the conventional GaAs MESFET having the same size as the embodiment.

EMBODIMENT 2

Atomic monolayers were grown, one layer by one layer, through the atomic-layer-controlled-epitaxy (ALE) method reported by Usui et al. in Japan Journal of Applied Physics Letter, Vol. 25, page 212 in 1986.

At first, a high-resistance GaAs layer (a part of 2 below 8 in Fig. 1) was grown on a semi-insulating GaAs substrate 1 to a thickness of 0.8 µm by the conventional VPE method. Then, by means of the ALE method, 35 layers of GaAs monolayers were grown on the high-resistance GaAs layer and one atomic monolayer of Se was grown at a sheet density of 1×10^{12} cm^{-2} to form the lower planar-doped layer 8. The GaAs monolayers 9 were grown again in number of 25 layers, and then Se was absorbed on the surface at a sheet density of 1×10^{12} cm^{-2} to form the upper planar-doped layer 7. Thereafter, the GaAs monolayers were grown in number of 110 layers and then ohmic electrodes 3 and 4 and a gate electrode 6 similar to those in the embodiment 1 were formed. In this device also, the mobility was 4000 cm^2/V·sec, considerably higher than the value of the conventional FET. In addition, it was possible to effect atomic scale control of the interval between the two-dimensionally doped

atomic layers 7 and 8 and there were great improvements in uniformity within the plane of the substrate and also in reproducibility. The cut-off frequency of the FET prepared in this way was also enhanced to 35 GHz beyond the value 20 GHz of the conventional GaAs MESFETs having the same configuration. The FET of the embodiment 2 was obtained with excellent reproducibility.

Claims

1. A compound semiconductor planar-doped field effect transistor characterized in that two planar-doped layers, each having two-dimensionally doped impurities, are provided within the channel region between the source and the drain at an interval substantially equal to or less than the mean free path of electrons.

2. A compound semiconductor field-effect transistor comprising a compound semiconductor substrate, a compound semiconductor channel region formed on said substrate, a source and a drain located on the opposite sides of said channel region, a gate electrode formed on said channel region, a first atomic planar-doped layer formed within said channel region at a first depth from the surface of said channel region and extending between said source and drain, and a second atomic planar-doped layer formed within said channel region at a second depth larger than said first depth from said surface of said channel region and extending between said source and drain in parallel with said first atomic planar-doped layer, the distance between said first and second atomic planar-doped layers being substantially equal to or less than the mean free path of electrons.

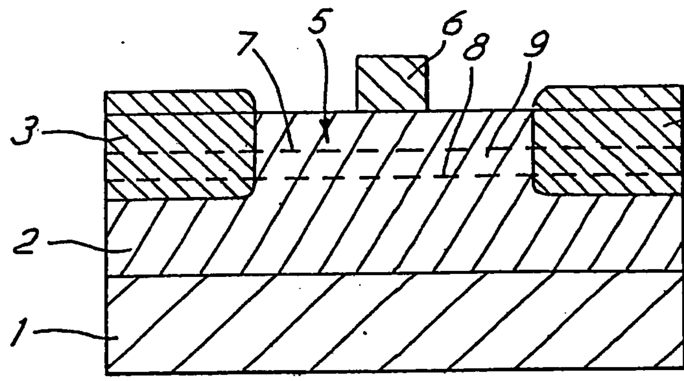

FIG.1

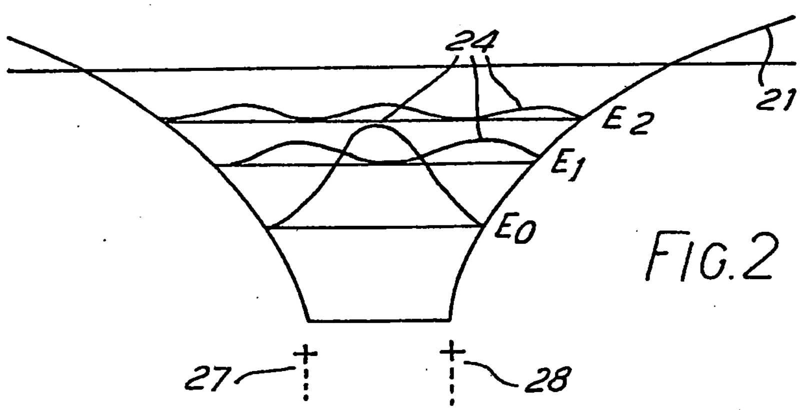

FIG.2

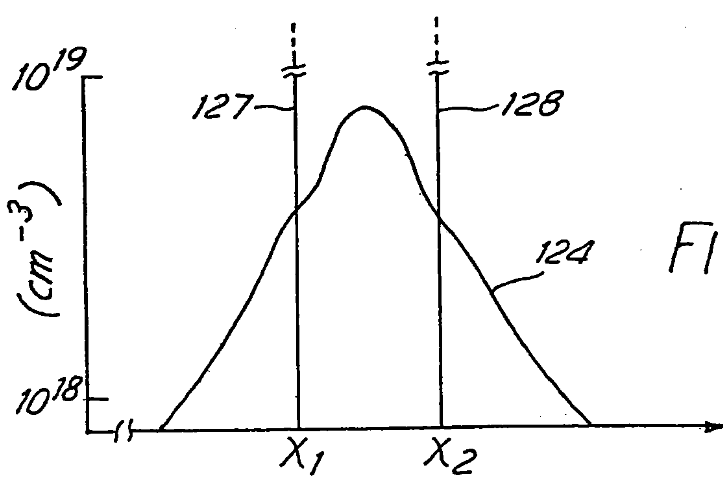

FIG.3

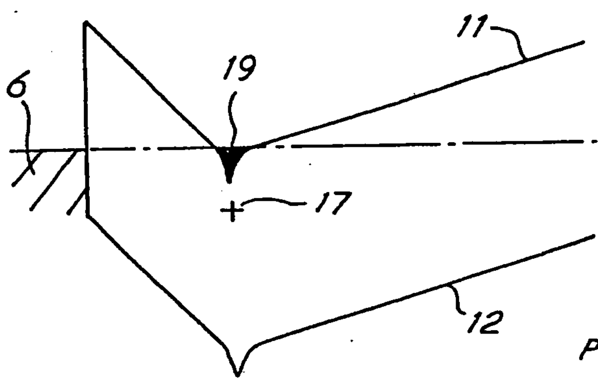

FIG. 4

PRIOR ART

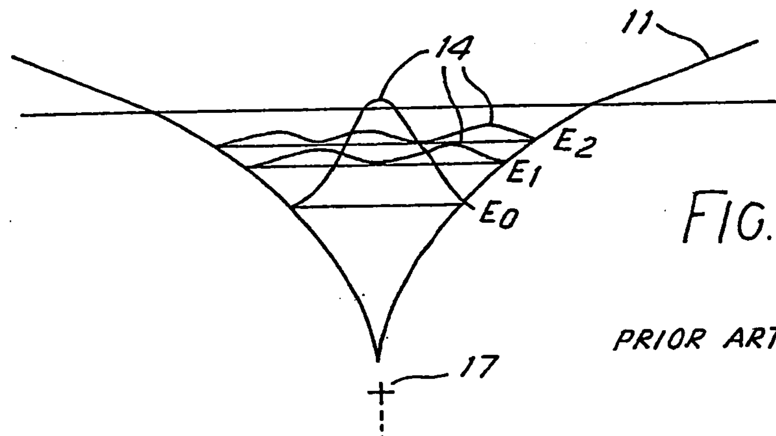

FIG. 5

PRIOR ART

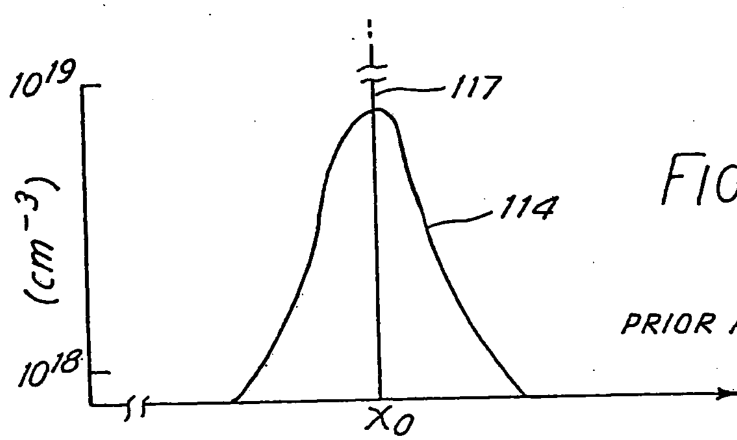

FIG. 6

PRIOR ART

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EUROPEAN SEARCH REPORT

Application Number

EP 88 30 8896

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EP-A-0 183 146 (MAX-PLANCK-GESELLSCHAFT ZUR FÖRDERUNG DER WISSENSCHAFTEN E.V.) * Page 15, line 26 - page 19, line 19; figures 1,1C * ---	1,2	H 01 L 29/36 H 01 L 29/80 H 01 L 29/10 // H 01 L 21/203 H 01 L 21/205
A	EP-A-0 196 245 (FUJITSU LTD) * Page 4, lines 4-17; page 8, line 15 - page 9, line 16 * -----	1,2	
			TECHNICAL FIELDS SEARCHED (Int. Cl.4)
			H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19-12-1988	MORVAN D.L.D.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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